A GaAs Integrated Circuit for Wideband Digital Quadrature Demodulation

R. J. Inkol
Defence Research Establishment Ottawa
Ottawa, Ontario
Canada, K1A 0Z4

V. Szwarc and L. Desormeaux
Communications Research Center
Ottawa, Ontario
Canada, K2H 8S2

M. Esonu and D. Al-Khalili
Royal Military College
Kingston, Ontario
Canada, K7L 5K0

Abstract

An integrated circuit has been designed to perform signal processing functions including digital quadrature demodulation on a sampled intermediate frequency signal in electronic warfare receivers. A -3 dB bandwidth exceeding 80 MHz is achieved using a fully pipelined, parallel architecture implemented on a GaAs gate array.

Introduction

Quadrature demodulation yields an efficient representation of the information contained in a bandpass IF signal and facilitates the extraction of amplitude and phase information. Analog quadrature demodulators are commonly used in radar, communications, and electronic warfare receivers although errors resulting from gain and phase imbalances between the inphase (I) and quadrature (Q) channels generally limit the attainable image rejection performance [1]. Although digital signal processing techniques have potential performance advantages, they have been generally considered impractical for bandwidths greater than a few tens of MHz. This paper describes an Application Specific Integrated Circuit (ASIC) intended to perform quadrature demodulation and other functions in electronic warfare receivers. It exploits advances in digital signal processing algorithms and microelectronics technology to achieve a -3 dB bandwidth exceeding 80 MHz.

ASIC Architecture

Figure 1 is a simplified block diagram of the ASIC. Digitized IF data from an 8 bit analog-to-digital converter (ADC) is translated to GaAs logic levels and processed by a digital quadrature demodulator. The I and Q signals are demultiplexed into even and odd data to halve the data rate, and translated to TTL logic levels. The I and Q data are also processed by the signal detection block to determine the presence of pulse signals having a useful signal-to-noise ratio. The buffer memory controller generates the address and control signals required to store the I and Q signal data immediately preceding, during, and following each pulse in a dual port static RAM. At the start of a pulse, a time stamp is generated by latching the output of a free running counter. The time stamp and address information required to access the I and Q signal data stored in the dual port RAM are stored in a separate external status FIFO memory. The signal data can be accessed for subsequent processing using straightforward memory mapped input/output techniques.

Digital Quadrature Demodulation Algorithm

Figure 2 shows the block diagram of a novel digital quadrature demodulation algorithm that has been evolved for implementation in special purpose hardware. It is conceptually similar to Rader's algorithm [2], but uses two highpass finite impulse response (FIR) filters having a relative phase shift of $\pi/2$. The digitized IF signal data is sampled at a rate f_s with the even and odd signal samples processed by separate filters. The pair of filters can be regarded as a complex bandpass filter. Consequently, DC offsets from the ADC are suppressed and the performance requirements for the analog IF filters preceding the ADC can be relaxed. The computational cost is minimized by implementing the I filter as a half-band filter having nearly half of its coefficients equal to zero and using decimation operations to reduce the output data rate to a value $f_s/4$ consistent with the filter bandwidths.

An important factor in determining the hardware cost of implementing the quadrature demodulation filters is the arithmetic precision required to achieve the desired error performance. An iterative search procedure was used to find sets of filter coefficients that achieve a favourable tradeoff between the number of nonzero digits in the signed magnitude binary representations of the filter coefficients and the flatness and matching of the passband frequency responses [3]. The set of 29 filter coefficients listed in Table I was selected. The odd and even coefficients are used in the inphase and quadrature filters, respectively. Of

the 23 nonzero coefficients, 18 coefficients have magnitudes represented by single fractional powers of 2. Consequently, the associated multiplication operations can be realized as hardwired bit shift operations. The 5 remaining coefficients can be represented by a sum of 4 or fewer fractional powers of 2.

The performance of the quadrature demodulator using the quantized filter coefficients compares favourably in passband flatness and phase error to that obtained using the floating point coefficients given by the Hamming window design method. The passband frequency responses of the I and Q channels are plotted in Figure 3 for the quantized filter coefficients. The phase error performance is determined by the quantization and other error mechanisms of the ADC. Simulations indicate a phase error of 0.1 (0.39) degrees RMS for ideal 8 (6) bit quantization over the Nyquist bandwidth $f_N=f_s/4$. Table II gives the image rejection ratio at several frequency offsets from the quadrature demodulator center frequency $f_{IF}=f_s/4$.

The quadrature demodulation filters are well suited for VLSI implementation. The transpose form architectures of the I and Q filters shown in Figure 4 utilize pipelining and parallelism to maximise throughput. Except for multiplexing and sample realignment, all clocking is performed at 1/4 of the rate f_s at which the IF signal is sampled. Although the quadrature filter does not make use of the symmetry properties of the filter coefficents to reduce the number of multipliers, this is not a problem since bit shift operations are used to implement all of the multiplication operations except those associated with coefficient h_{13}. By reordering the arithmetic only a single multiplier is required.

Implementation

The ASIC was designed using the Vitesse FX gallium arsenide (GaAs) gate array technology [4]. The gate array design methodology minimises risk and design effort. There are some penalties in chip area and performance, but these were found to be acceptable. The GaAs technology was selected because of its high speed, moderate power consumption, and the availability of ECL and TTL compatible I/O buffers on the same device.

MATLAB, LASAR and proprietary Vitesse tools in a Mentor Graphics environment were used in the design of the ASIC. Functional verification of the quadrature demodulator operation involved simulating the algorithm and the schematic level representation of the hardware implementation using MATLAB and QUICKSIM, respectively. Test files of sampled and quantized sinusoidal signals generated in the appropriate formats for MATLAB and QUICKSIM were processed and the resultant output signals were compared using time and frequency domain signal representations. Due to rounding used in the ASIC design to reduce hardware complexity and the input/output (I/O) pin count, there were some differences, but these were not significant.

Vitesse tools were used for front, intermediate and back annotations, followed by post routing simulation using QUICKSIM. The same tools were used for placement and test vector generation. A further layer of timing verification was performed for normal and extreme conditions using the LASAR simulator to detect potential timing hazards resulting from on-chip skews.

Careful design optimization was necessary to achieve the performance goals. Important design issues concerned the generation and distribution of the master clock signal, the performance optimization of critical functional blocks such as multipliers, and the application of pipelining.

Both the single phase 100 MHz master clock used by the major portion of the logic blocks and a 50 MHz clock for controlling data output are generated by a modified divide by 8 Johnson counter. Provisions are made for synchronizing the operation of the clock generator logic in multiple devices. The 100 MHz clock is distributed by a H-tree clock distribution network to minimise clock skews. The multipliers were implemented using hard wired shift and add/subtract operations. This is more economical in hardware than using a conventional array multiplier since a multiplication by a quantized filter coefficient can be performed with a maximum of 3 addition and subtraction operations. Pipeline registers were inserted between each pair of cascaded adders and after each multiplier.

The inclusion of built-in-self-test (BIST) circuitry permits the internal circuitry of the ASIC to be tested at clock frequencies exceeding 400 MHz using a minimum of test equipment. Provisions are made for applying test vectors generated by a linear feedback shift register (LFSR) to the quadrature demodulator input. In addition, a second LFSR generates test vectors to exercise the control circuitry. The outputs of the data and address ports are routed to a multiple input LFSR based compactor circuit whose signature is compared to the expected result.

Results

The design has been completed and simulated. Table III gives the cell counts of the major functional blocks (1 cell = 2-input NOR gate). Approximately 35,200 of the 102,272 internal cells contained on a 320 x 280 mil die are used, resulting in an estimated power dissipation of ~9.1 W. Simulation results corresponding to worst case commercial conditions with estimated wire delays indicate that the multipliers will have typical delays of less than 3 ns and that the ASIC will operate at a typical clock frequency in excess of 500 MHz. At this sampling rate, the -3 dB bandwidth would exceed 100 MHz, more than 5 times greater than the bandwidth of the quadrature demodulator reported in [5].

Table I. Quantized Filter Coefficients

Filter Coefficients in Powers of 2
$h_0=h_{28}=-2^{-8}$
$h_1=h_{27}=-2^{-7}$
$h_2=h_{26}=0.0$
$h_3=h_{25}=2^{-6}$
$h_4=h_{24}=2^{-5}$
$h_5=h_{23}=2^{-5}$
$h_6=h_{22}=0.0$
$h_7=h_{21}=-2^{-4}$
$h_8=h_{20}=-2^{-3}$
$h_9=h_{19}=-2^{-3}$
$h_{10}=h_{18}=0.0$
$h_{11}=h_{17}=2^{-2}$
$h_{12}=h_{16}=2^{-1}+2^{-5}+2^{-6}+2^{-8}$
$h_{13}=h_{15}=2^{0}-2^{-3}-2^{-4}-2^{-7}$
$h_{14}=2^{0}-2^{-3}+2^{-5}$

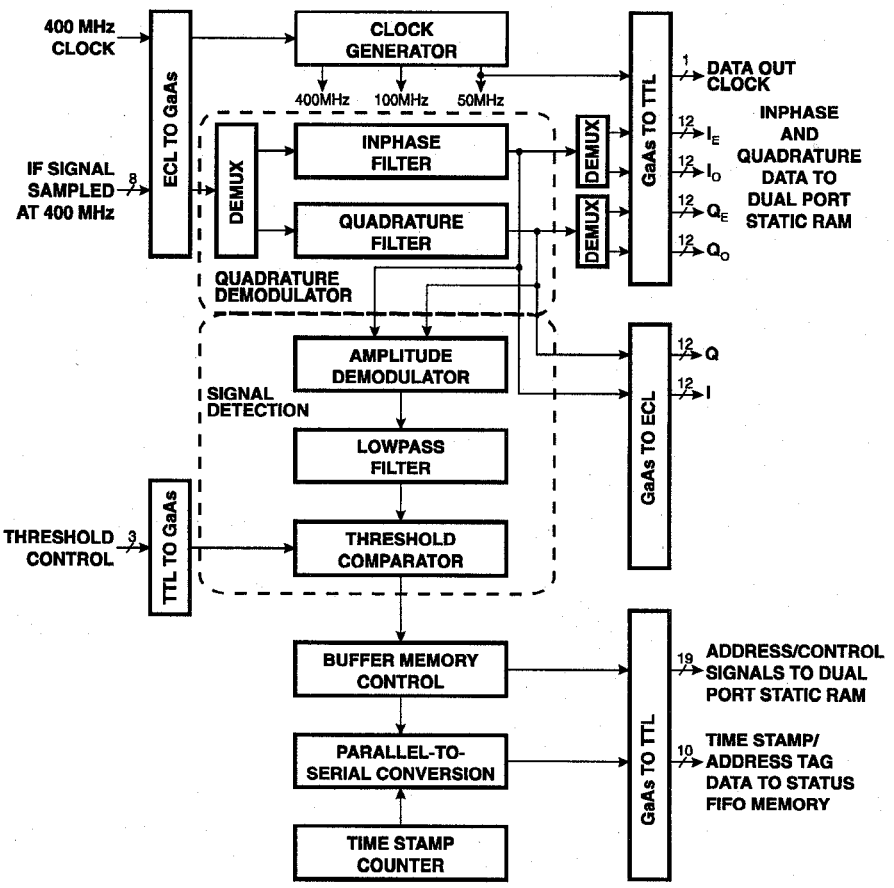

Figure 1. Simplified architecture of application specific integrated circuit.

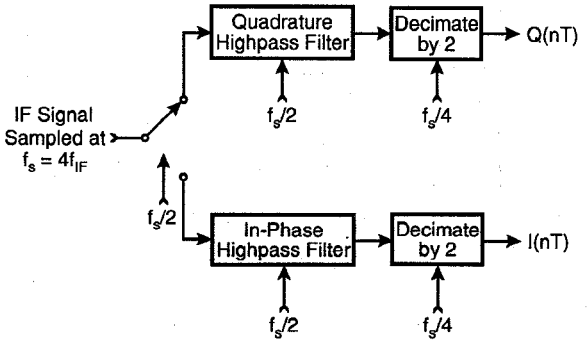

Figure 2. Digital quadrature demodulation algorithm. The IF center frequency f_{IF} and Nyquist bandwidth are fixed at one quarter of the sampling rate f_s.

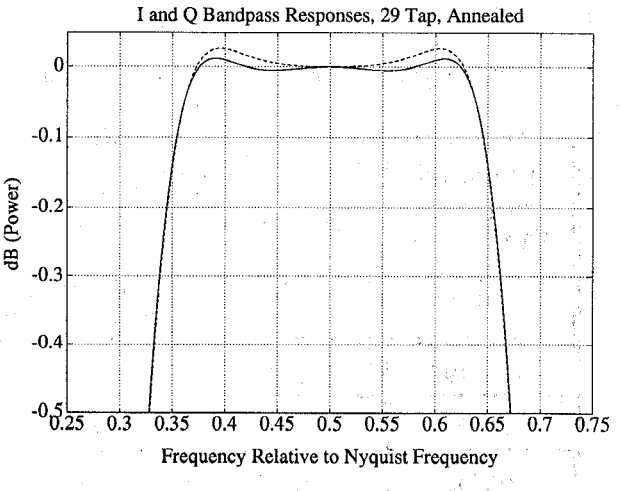

Figure 3. Bandpass equivalent frequency responses of inphase (solid line) and quadrature (dashed line) filters.

References

[1] D. L. Sharpin et al., "The Effects of Quadrature Sampling Imbalances on a Phase Difference Analysis Technique," Proc. of 1990 National Aerospace Electronics Conf., May 1990.

[2] C. M. Rader, "A Simple Method for Sampling In-phase and Quadrature Components," IEEE Trans. AES, VOL. 20, NO. 6, Nov. 1984.

[3] R. J. Inkol and M. Herzig "An Efficient Digital Quadrature Demodulator," Symp. on Communications, Queens University, May 1994.

[4] FX Family Gate Array Design Manual, Version 3.0, Vitesse Semiconductor Corporation, Dec. 1992.

[5] S. L. SanGregory and M. A. Mehalic, "A 2K x 8-bit Single Chip Digital Radio Frequency Memory," Proc. of 1993 ASIC Conf., Sept. 1993.

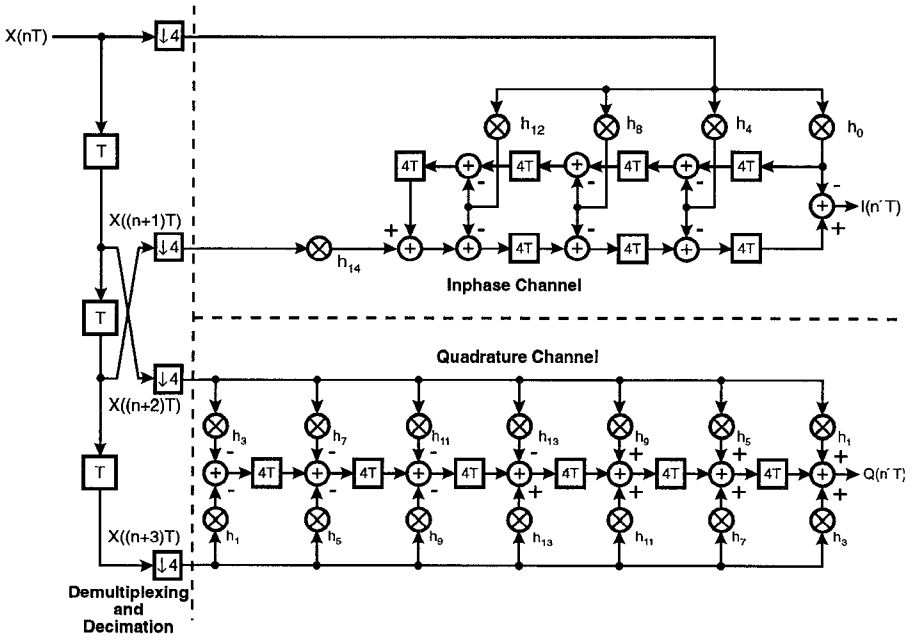

Figure 4. Inphase and quadrature demodulation filters.

Table II. Quadrature Demodulator Image Rejection

Normalized Frequency Offset from f_{IF} (f_N=±0.5)	Image Rejection Ratio in dB	
	Quantized Filter Coeff.	Hamming Window Filter Coeff. (Floating Point)
±0.00195	132.3	56.3
±0.125	62.4	56.6
±0.250	67.9	57.6
±0.375	64.5	58.5

Table III. Cell Count of Major Functional Blocks

Functional Block	Cell Count
Clock Generator	184
ADC Interface	834
1 to 4 Demultiplexer	2,580
Inphase Filter	9,392
Quadrature Filter	7,790
Signal Detection	8,665
Built In Self Test	1,074